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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PRUCHNIC, STANLEY J	
ART UNIT	PAPER NUMBER
2859	

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,535	ASLAN ET AL.	
	Examiner	Art Unit	
	Stanley J. Pruchnic, Jr.	2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 29 September 2005 with respect to claims 1-20 have been fully considered. Applicant's arguments have been addressed as applied to the amended claims.

2. Applicant's argument with respect to the rejection of Claims 1, 3, 6, 8, 10, 13, 15, 17 and 20 under 35 U.S.C. 102(e) as being anticipated by US 20040001527 A1 (Grannes, Dean J. *et al.*, GRANNES), to summarize, is that, in the disclosure of GRANNES, the "diodes are not collocated". In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (*i.e.*, **diodes** that are "collocated") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claims require only that the "dual diode **system**" ... "is collocated on a first substrate" and GRANNES discloses a distribution of diodes comprising more than one "dual diode system", each such system being "collocated on a first substrate" as more fully described in the rejection *infra*. Moreover, because the diode systems are collocated on a first substrate, the temperature of the first substrate is more accurately determined, in contrast to a substrate that only has one or two diodes located thereon.

3. Applicant's argument (beginning on Page 6 of the "REMARKS/ARGUMENTS" received 29 September 2005), with respect to the rejection of Claims 2, 9 and 16 under 35 U.S.C. 103 (a) as being unpatentable over GRANNES in view of US 5195827 A (Audy; Jonathan M. *et al.*, AUDY) is not persuasive as described above.

4. Applicant's argument (on Page 7 of the "REMARKS/ARGUMENTS" received 29 September 2005), with respect to the rejection of Claims 4-5, 11-12 and 18-19 under 35 U.S.C. 103 (a) as being unpatentable over GRANNES is not persuasive as described

above, as applied to the amended claims, but Applicant's argument regarding the rejection of ***Claims 4, 11 and 18*** is **persuasive** as applied to the amended claims.

Applicant argues that GRANNES fails to teach or suggest a dual diode system having a bias circuit that is formed on the first substrate, because GRANNES discloses the temperature measurement circuit is on the second substrate and not the first substrate and motivation is lacking for shifting the position of the bias circuit.

In response, it is noted that although GRANNES further disclosed that the temperature sensing circuit 230 is alternatively manufactured on the same die as integrated circuit 100 (Fig. 2; Paragraph [0027]), in that embodiment, as disclosed by GRANNES, the bias circuit would also be on the first substrate, now considered to be teaching away from the temperature measurement circuit being formed on a second substrate as claimed by Applicant, in combination with the remaining limitations of the claim(s).

5. Applicant's argument (on Page 7 of the "REMARKS/ARGUMENTS" received 29 September 2005), with respect to the rejection of Claims 1-2, 4, 7-9, 11, 13-16, 18 and 20 under 35 U.S.C. 103(a) as being unpatentable over US 5,982,221 A (TUTHILL) in view of US 6,612,738 B2 (Beer; Peter *et al.*, BEER) is not persuasive as described above, as applied to the amended claims. Applicant's argument that the motivation is "too general" because it contemplates any invention that saves space and using a second substrate for measurements is not persuasive since BEER shows that it is well known to provide the measurement circuitry "off-chip". See also US 5639163 A (Davidson; Evan Ezra *et al.,* DAVIDSON), US 6008685 A (Kunst; David J., KUNST), US 4791380 A (Chiappetta; Joseph F., CHIAPPETTA), US 6480127 B1 (Aslan; Mehmet, hereinafter ASLAN'127), US 6332710 B1 (Aslan; Mehmet et al., hereinafter ASLAN'710), and US 6097239 A (Miranda, Jr.; Evaldo Martino *et al.*, MIRANDA).

Claim Objections

6. Claims 16-20 are objected to because of the following informalities: in each of claims 16-20, in the first line of the preamble, "method" should be deleted and replaced therefor by –system-- in order to more clearly describe the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. **Claims 1, 3, 6, 8, 10, 13, 15, 17 and 20** are rejected under 35 U.S.C. 102(e) as being anticipated by US 2004/0001527 A1 (Grannes, Dean J. *et al.*, hereinafter **GRANNES**).

With respect to **Claims 1, 3, 8, 10, 15 and 17**: GRANNES discloses a system (Figs. 1-2) and method (Steps 310-350) for measuring temperatures of a device, as claimed by Applicant, comprising:

a dual diode system that is collocated on a first substrate 100. GRANNES discloses first substrate 100 includes more than one "dual diode system" on the same substrate, broadly considered "collocated" as claimed by Applicant in each of Claims 1, 8 and 15. A "dual diode system" is comprised of diode pairs, or "dual diodes", each pair being a "dual diode system" associated with three terminals, *i.e.,* see paragraph 20, which may be implemented as bumps or pins.

GRANNES further discloses a dual diode system comprises a first terminal (*e.g.*, 121) that is coupled to a first electrode of a first junction diode 105 (and further regarding **Claims 3, 10 and 17**, the first electrode of the first junction diode 105 comprises a cathode), wherein the first electrode of the first junction diode 105 has a first polarity as claimed by Applicant in Claim 1 (the cathode considered to have a "negative" polarity, as is conventional).

GRANNES further discloses the dual diode system comprises a second terminal (122) that is coupled to a first electrode of a second junction diode 103, wherein the first electrode of the second junction diode 103 has the first polarity (and further regarding **Claims 3, 10 and 17**, the first electrode of the second junction diode 104 also comprises a cathode, having the same polarity, both being cathodes).

GRANNES further discloses the dual diode system comprises a third terminal (123) that is coupled (shown in Fig. 1 as a direct connection) to second electrodes of the first and second junction diodes, wherein the second electrodes of the first and second junction diodes have a second polarity that is opposite of the first polarity (and further regarding **Claims 3, 10 and 17**, the second electrodes of the first and second junction diodes each comprise an anode), each having the opposite polarity of the cathode, which is, following the convention above, considered a "positive" polarity.

GRANNES further discloses (Fig. 2) the dual diode system comprises a temperature measurement circuit (230) that is collocated on a second substrate (Fig. 2; see Paragraphs [0021-0022], and that is configured to perform a voltage measurement ("diode measurements") using at least one of the first and second terminals (which are the sources of signals 210 and 220), and regarding the method, performing a voltage measurement across the selected diode's terminals (step 340); and

GRANNES further discloses the dual diode system comprises a bias circuit that is configured to bias the third terminal 123. See Paragraph [0021], which discloses that voltages applied to a selected diode will cause current to flow through that diode when it is forward biased, *e.g.*, consistent with the above, the diode 105 will be forward biased

when the cathode terminal (121) is at a higher voltage (at least 0.7 volts) than the anode terminal (123). Although the bias circuit is not explicitly shown, it is inherent from the disclosure that terminal 123 is biased by a bias circuit whenever GRANNES selects diode 105, as claimed by Applicant, that is, whenever a known current is sent through diode 105 (Step 330 in Fig. 3).

Further regarding **Claim 6**, GRANNES discloses the temperature measurement circuit is configured to perform a voltage measurement using the third terminal.

Further regarding **Claims 13 and 20**, both first and second terminals are used for measurement of a voltage across a selected diode (*e.g.*, for either of diodes 101 and 102).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. **Claims 2, 9 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over GRANNES in view of US 5,195,827 A (Audy; Jonathan M. et al., hereinafter **AUDY**).

GRANNES, to summarize, discloses all the limitations as claimed by Applicant in **Claims 2, 9 and 16** as described above in Paragraph 8 as applied to **Claims 1, 3, 6, 8, 10, 13, 15, 17 and 20,** further including the disclosure that "a diode" of the system of GRANNES is typically implemented as the base-emitter junction of a substrate connected PNP transistor (Paragraph [0004].

GRANNES does not explicitly disclose the limitations wherein the first electrode of the second junction diode comprises an emitter, and the second electrodes of the first and second junction diodes each comprise a base.

AUDY relates to the art of temperature measurement on integrated circuit devices having a substrate.

AUDY teaches that bipolar transistors (either NPN or PNP) and diodes are art-recognized equivalent p-n junction devices for measuring temperature on substrates using the forward-bias diode equation. Although AUDY illustrates the equivalence using an NPN transistor (Figs. 1-2), AUDY teaches that the same applies to PNP transistors (Col. 3, Lines 40-60). Moreover, AUDY teaches that substituting a bipolar transistor for a diode is advantageous since the bipolar transistor tends to give more accurate temperature measurement results (Col. 6, Lines 23-30).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a PNP bipolar transistor for the junction diodes of GRANNES as already taught by GRANNES, and in so doing, the first electrode of the second junction diode would comprise an emitter, and the second electrodes of the first and second junction diodes would each comprise a base as taught by AUDY, because they are art recognized equivalents and since the bipolar transistor tends to give more accurate temperature measurement results as taught by AUDY.

12. **Claims 5, 12 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over GRANNES.

GRANNES, to summarize, discloses all the limitations as claimed by Applicant in **Claims 5, 12 and 19** as described above in Paragraph 8 as applied to **Claims 1, 3, 6, 8, 10, 13, 15, 17 and 20,** further including the disclosure that the dual diode system comprises a bias circuit that is configured to bias two terminals at one time (in order to apply a current) while leaving the other terminals in a high impedance state so that no current flows through those (Paragraph [0021]). GRANNES does not explicitly state that the bias circuit is formed on one of the second substrate, a third substrate, and a discrete component as claimed by Applicant in Claims 5, 12 and 19.

As described above, GRANNES requires each of the terminals on the semiconductor substrate (die) to be capable of having a current impressed by the measurement circuitry when a given diode is selected for temperature measurement and GRANNES at least suggests that each of the terminals should be in a high impedance state when not being biased, in order to not have a current flowing there-through, in order to not interfere with a measurement of voltage across a selected two terminals. Because all the terminals are held in a high impedance state as the default condition, as suggested by GRANNES, each of the terminals are accessible from the second substrate 230, the bias would normally be applied from a means external to the first substrate, the second substrate 230.

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the bias circuit on the second substrate as suggested by GRANNES, instead of on the first substrate, in the case where the sensing circuit is on the second substrate, in order that the sensing circuit would have direct control over the application of the currents that bias the desired terminals as already suggested by GRANNES.

13. **Claims 1-2, 4, 7-9, 11, 13-16, 18 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,982,221 A (Tuthill; Michael G., hereinafter **TUTHILL**) in view of US 6,612,738 B2 (Beer; Peter et al., hereinafter **BEER**).

TUTHILL discloses or suggests a system and method for measuring temperatures of a device, comprising:

a dual diode (*e.g.,* diode-connected transistors) system (Fig. 3; Col. 2, Lines 26-28) that is collocated on a first substrate and that has a first terminal (C1; capacitor 70) that is coupled to a first electrode (labeled 1) of a first junction diode Q1 (68), wherein the first electrode of the first junction diode Q1 has a first polarity, a second terminal (C2; capacitor 72) that is coupled to a first electrode (labeled 1) of a second junction diode Q2 (66), wherein the first electrode of the second junction diode Q2 has the first polarity (both are emitters as claimed by Applicant in **Claims 2, 9 and 16**, having the same polarity) and a third terminal that is coupled (AGND) to second electrodes of the first and second junction diodes (each comprise a base as claimed by Applicant in **Claims 2, 9 and 16**), wherein the second electrodes of the first and second junction diodes have a second polarity that is opposite of the first polarity;

a temperature measurement circuit (op-amp 78) that is formed on a substrate and that is configured to perform a voltage measurement using at least one of the first and second terminals (using both) ; and

a bias circuit (*i.e.*, being *grounded*) that is configured to bias the third terminal.

Further regarding **Claims 4, 11 and 18**: the bias circuit is formed on the first substrate, considering the current sources are part of the bias circuit.

Further regarding **Claims 7 and 14:** TUTHILL discloses the temperature measurement circuit comprises a differential analog-to-digital converter, the differential input of the amplifier being considered the "front end" of the differential analog-to-digital converter.

TUTHILL discloses the differential amplifier outputs a voltage related to temperature. Moreover, (Col. 5) TUTHILL's disclosure anticipates adding an analog-to-digital converter to the differential amplifier in order to convert the output voltage to a digital value. The output is typically measured by a 10-bit analog to digital converter with

a 2.5 Volt reference and should have a sensitivity of 0.25 degrees per least significant bit (LSB) or four LSB's per degree, for example, in order to meet requirements of a temperature sensor, providing a digital output.

Further regarding **Claims 13 and 20**, both first and second terminals are used for measurement of a voltage.

TUTHILL does not disclose the temperature measurement circuit (op-amp 78) is formed on a ***second substrate*** as claimed by Applicant in each of the independent claims 1, 8 and 15.

BEER relates to the art of temperature measurement on integrated circuit devices having a substrate.

BEER teaches forming a temperature measurement circuit on a second substrate, apart from the first substrate having thermal diodes for measuring temperature of the first substrate in order to use the measurement circuit for testing semiconductor devices in a test mode (Col. 3, Lines 5-54; *e.g.*, Lines 29-36).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the temperature measurement circuit on a second substrate as taught by BEER instead of on the same substrate as done by TUTHILL in order to provide more available space on the first substrate and making the second substrate usable for testing a plurality of first substrates at different times.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art cited in a previously sent form PTO-892 and not mentioned above disclose related temperature measurement devices and methods and diode structures.

- US 6097239 A (Miranda, Jr.; Evaldo Martino et al., hereinafter MIRANDA), US 6008685 A (Kunst; David J., hereinafter KUNST), US 6554469 B1 (Thomson; David

et al., hereinafter THOMSON), US 6480127 B1 (Aslan; Mehmet, hereinafter ASLAN'127), and US 6332710 B1 (Aslan; Mehmet et al., hereinafter ASLAN'710) disclose single diodes with sequential excitation.

- US 5639163 A (Davidson; Evan Ezra et al., hereinafter DAVIDSON), US 4791380 A (Chiappetta; Joseph F., hereinafter CHIAPPETTA), US 6726361 B2 (Bisping; Michael et al., hereinafter BISPING), and US 5094546 A (Tsuji; Takahiro, hereinafter TSUJI) disclose "matched pair" type thermal diodes for temperature measurements on chips.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanley J. Pruchnic, Jr., whose telephone number is **(571) 272-2248**. The examiner can normally be reached on weekdays (Monday through Friday), the best hours being from 8:30 AM to 4:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez (Art Unit 2859) can be reached at **(571) 272-2245**. The Central FAX Number for *all official USPTO communications* is **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application or proceeding may be directed to the official USPTO website at **http://www.uspto.gov/** or you may call the **USPTO Call Center** at **800-786-9199** or 703-308-4357. The Technology Center 2800 Customer Service FAX phone number is (703) 872-9317.

The cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources.

Private PAIR provides external customers Internet-based access to patent application status and history information as well as the ability to view the scanned images of each customer's own application file folder(s).

For inquiries relating to Patent e-business products and service applications, you may call the *Patent Electronic Business Center (EBC)* at 703-305-3028 or toll free at 866-217-9197 between the hours of 6 a.m. and midnight Monday through Friday EST, or by e-mail at: **ebc@uspto.gov**. Additional information is available on the Patent EBC Web site at: **http://www.uspto.gov/ebc/index.html**.

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Stanley J. Pruchnic, Jr.
10/25/05